

Design and Implementation of an Educational Resource for Teaching Network Topologies

Diseño e implementación de un recurso educativo para la enseñanza de topologías de red

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Abstract

Introduction: The teaching of computer network topologies often involves abstract concepts that can be difficult for students to understand through theoretical explanations alone. In this context, interactive educational resources based on low-cost electronic components can support the visualization of communication structures and data flow.

Objective: To design and implement an interactive educational resource for teaching star and ring network topologies using Arduino UNO microcontrollers, LEDs, push buttons, and low-cost electronic components.

Method: A didactic and experimental approach was employed through the development of two functional prototypes. The first prototype represented the star topology using centralized control logic, while the second simulated the ring topology through a sequential transmission process between nodes. Both prototypes were designed to allow students to physically and visually observe the behavior of each network structure.

Results: The results showed that the system clearly represented the flow of information in both topologies. The

star topology prototype demonstrated the dependence on a central node, whereas the ring topology prototype illustrated the sequential circulation of data among nodes. Additionally, the resource proved to be low-cost, replicable, and useful for strengthening basic electronics, embedded programming, and network architecture skills.

Conclusions: The proposed prototype constitutes a technically functional, low-cost, and replicable educational resource with pedagogical potential for supporting the understanding of abstract network concepts. Its impact on student learning outcomes should be further validated through controlled pedagogical studies.

Keywords

Arduino; Network Topologies; Star Topology; Ring Topology; Educational Technology

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Resumen

Introducción: La enseñanza de las topologías de redes de computadores suele involucrar conceptos abstractos que pueden resultar difíciles de comprender mediante explicaciones teóricas únicamente. En este contexto, los recursos educativos interactivos basados en componentes electrónicos de bajo costo pueden apoyar la visualización de las estructuras de comunicación y del flujo de datos.

Objetivo: Diseñar e implementar un recurso educativo interactivo para la enseñanza de las topologías de red en estrella y en anillo, utilizando microcontroladores Arduino UNO, LEDs, pulsadores y componentes electrónicos de bajo costo.

Método: Se empleó un enfoque didáctico y experimental mediante el desarrollo de dos prototipos funcionales. El primer prototipo representó la topología en estrella a través de una lógica de control centralizada, mientras que el segundo simuló la topología en anillo mediante un proceso de transmisión secuencial entre nodos. Ambos prototipos fueron diseñados para permitir que los estudiantes observaran física y

visualmente el comportamiento de cada estructura de red.

Resultados: Los resultados mostraron que el sistema representó claramente el flujo de información en ambas topologías. El prototipo de topología en estrella evidenció la dependencia de un nodo central, mientras que el prototipo de topología en anillo ilustró la circulación secuencial de los datos entre nodos. Además, el recurso demostró ser de bajo costo, replicable y útil para fortalecer habilidades en electrónica básica, programación embebida y arquitectura de redes.

Conclusiones: El prototipo propuesto constituye un recurso educativo técnicamente funcional, de bajo costo y replicable, con potencial pedagógico para apoyar la comprensión de conceptos abstractos de redes. Su impacto en los resultados de aprendizaje de los estudiantes deberá validarse posteriormente mediante estudios pedagógicos controlados.

Palabras clave

Arduino; Topologías de red; Topología Estrella; Topología Anillo; Tecnología Educativa

INTRODUCTION

Network topologies are an essential element in the study of communications and network architecture, as they determine how nodes interconnect, exchange information, and respond to failures or variations in data flow. In this context, star and ring topologies represent classic configurations widely used to explain principles of connectivity, centralization, sequentiality in transmission, and the structural organization of a network [1], [2]. Their study is not only relevant from a technical perspective, but also from an educational standpoint, as they form the basis for understanding more complex architectures used in institutional, business, and technological environments [3], [4].

Several studies have shown that network topology can be analyzed as a key tool in information, communication, and monitoring systems, due to its influence on infrastructure efficiency, control, and performance [2], [3]. Likewise, recent research confirms that interest in network topologies remains relevant in emerging fields such as the Medical Internet of Things (IoMT), where the selection of an appropriate architecture affects the reliability and distribution of connected devices [5]. Similarly, applied studies in educational and institutional contexts have developed proposals for data network implementation, communication systems, and connectivity prototypes, confirming the need to strengthen the practical understanding of these concepts from early stages of technical and technological training [6] – [8].

Despite their importance, the teaching of network topologies tends to remain predominantly theoretical, supported by abstract explanations, static diagrams, or conceptual descriptions that, in many cases, limit meaningful knowledge acquisition by students. This situation can lead to difficulties in interpreting the actual behavior of data transmission, node dependencies, and the functional differences between a centralized topology such as the star and a sequential topology such as the ring. Consequently, it is necessary to incorporate active educational methodologies that allow these contents to be transferred to concrete experimentation scenarios.

In this sense, the implementation of didactic resources based on electronic prototyping and hands-on laboratories constitutes a relevant strategy for strengthening teaching and learning processes. Experiences focused on the development of laboratories for teaching electronic technologies using Arduino demonstrate that experimental environments promote direct interaction with devices, visualization of system behavior, and the consolidation of technical competencies in students [9]. From this perspective, the use of physical assemblies to represent network topologies allows not only explaining the structure of communication, but also tangibly observing signal circulation, central node dependency, or the continuity of links between nodes.

Based on the above, this work proposes the implementation of star and ring network topologies through an educational methodology supported by physical and experimental resources, with the aim of facilitating the understanding of their operating principles in training contexts. The proposal articulates fundamentals of network architecture with a didactic strategy oriented toward active learning, encouraging students to connect theory with practice through observation, construction, and analysis of each topology's behavior. In this way, the article contributes an applied experience that strengthens the teaching of networks in academic settings, particularly in programs with a technological and engineering focus.

CONTRIBUTIONS

The main contribution of this study lies in the development of a prototyping-based educational methodology for teaching network topologies through a physical and interactive implementation supported by microcontroller programming. Unlike traditional approaches focused solely on theoretical explanation, the proposed strategy enables students to understand abstract network concepts through direct observation, system manipulation, and hands-on experimentation.

Specifically, this work contributes in three main areas. First, it presents a functional educational prototype that visually and dynamically represents the behavior of star and ring topologies, facilitating the understanding of communication flow, node interaction, and structural differences between both architectures. Second, it proposes an active learning methodology that links network theory with electronics and embedded programming, fostering deeper conceptual understanding and enabling the identification of learning gaps during the experimental process. Third, it offers a low-cost, scalable, and replicable didactic resource with implementation potential in engineering and technology training contexts to strengthen practical laboratory instruction.

Consequently, the novelty of this study is not limited to the technical construction of the prototype but extends to its pedagogical value as a didactic tool with potential to support student engagement, practical reasoning, and meaningful learning in computer network education. Empirical verification of this impact constitutes a future line of work to be addressed through.

MATERIALS AND METHODS

The experimental phase was grounded in an applied technological design that allowed merging theoretical concepts of network infrastructure with tangible physical implementations [10], [14]. This methodological approach was broken down into a logical sequence comprising three iterative stages: hardware architecture design, synchronization algorithm coding, and functional validation through real hardware simulation, enabling an empirical contrast between communication theory and the behavior of electrical signals in a controlled environment [5]. By using open-source microcontrollers, the transparency of logical processes and the possibility of replicating the experimental scenario with scientific precision were ensured, in accordance with rapid prototyping standards [11], [13].

A. Technical Specifications of the Hardware and Software Ecosystem

The technical ecosystem was configured using two Arduino Uno microcontrollers, selected for their stability in asynchronous signal processing and their ability to efficiently integrate serial communication protocols [11], [13]. The physical support was based on a large-format breadboard with 3,260 connection points, which facilitated an organized spatial distribution of nodes, minimizing electromagnetic interference and ensuring the integrity of physical links during traffic simulation [13], [15]. Light signaling was categorized using high-intensity LEDs (blue for the star topology and red for the ring topology) thereby achieving immediate pedagogical distinction in the observation of information packet transit [15].

Electrical protection of the microcontrollers was ensured by installing 220-ohm carbon resistors for actuators and 10-kilohm resistors in pull-down configuration to stabilize input signals, filtering accidental voltage noise in sensors and buttons [13]. The coding process was carried out in the official Arduino development environment using C++, implementing timing routines and event management functions that accurately emulate the behavior of a professional data network through previously validated synchronization protocols [12], [14].

TABLE 1. DETAILED MATERIALS BUDGET.

No.	Item	Price (COP)
1	Protoboard	68,900
2	Arduino UNO (2 units)	60,000
3	Jumper cables (pack x 40)	8,000
4	220-ohm resistors (pack x10)	600
5	Push buttons (2 units)	600
6	LED strip (1 meter)	11,400
7	LEDs (pack x 10)	3,000
8	LED display	14,000

Total	166,500
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B. Experimental Procedure

The star topology assembly consisted of creating a central node configured as an information flow manager or hub [10]. The first step was mapping five digital pins to peripheral terminals represented by blue LEDs, which are activated upon a specific input instruction [11], [15]. Subsequently, a listening routine was programmed that activates upon receiving an input pulse, executing a sequential activation sequence that simulates packet transmission from a server to its clients, validating the hierarchical dependency model described in the technical literature, where an interruption at the central node disables the entire network [10], [15]. (see Figure 1).

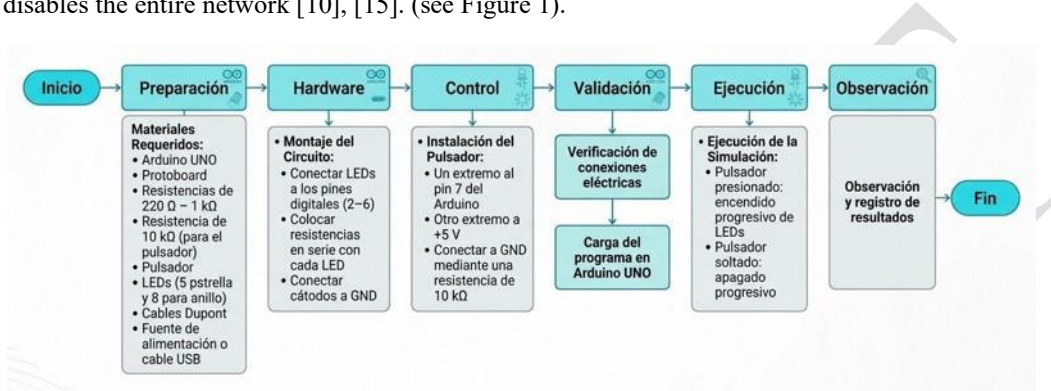


Figure 1. Flowchart of the experimental procedure and system operation.

For the ring topology, a closed circuit of eight serially interconnected nodes was structured, forming a circular data bus consistent with deterministic architectures [10]. A motion sensor was integrated to act as the system trigger, simulating the detection of incoming packets in the network [15]. The implemented algorithm manages the transit of a virtual token, which must travel through each point of the network before returning to the origin, allowing measurement of flow continuity and the intrinsic latency that occurs when the signal is processed by multiple intermediate stations before reaching its final destination [12], [14].

To provide greater robustness to this section, it is recommended to integrate visual elements that facilitate replication of the experiment [14]. This includes a pin assignment table specifying the exact connection of each component, a flowchart explaining the signal lifecycle from initial detection to completion of the illumination sequence, and a schematic diagram of the electrical connections, all of which will lend a professional and rigorous character to the methodology [11], [13]. (see Figure 2).

```

**Código A: Lógica para 5 LEDs**
const int led1Pin = 2; // LED 1 en pin 2
const int led2Pin = 4; // LED 2 en pin 4
const int led3Pin = 5; // LED 3 en pin 5
const int led4Pin = 6; // LED 4 en pin 6
const int led5Pin = 7; // LED 5 en pin 7 (nuevo)
const int buttonPin = 3; // Botón en pin 3

void setup() {
  pinMode(led1Pin, OUTPUT);
  pinMode(led2Pin, OUTPUT);
  pinMode(led3Pin, OUTPUT);
  pinMode(led4Pin, OUTPUT);
  pinMode(led5Pin, OUTPUT);
  pinMode(buttonPin, INPUT);
}

void loop() {
  int buttonState = digitalRead(buttonPin);
  if (buttonState == HIGH) {
    digitalWrite(led1Pin, HIGH);
    delay(500);
    digitalWrite(led2Pin, HIGH);
    delay(500);
    digitalWrite(led3Pin, HIGH);
    delay(500);
    digitalWrite(led4Pin, HIGH);
    delay(500);
    digitalWrite(led5Pin, HIGH);
  } else {
    digitalWrite(led5Pin, LOW);
    delay(500);
    digitalWrite(led4Pin, LOW);
    delay(500);
    digitalWrite(led3Pin, LOW);
    delay(500);
    digitalWrite(led2Pin, LOW);
    delay(500);
    digitalWrite(led1Pin, LOW);
  }
}

**Código B: Lógica para 8 LEDs con Bucle 'for**
const int leds[] = {2, 4, 5, 6, 7, 8, 9, 10};
// Pines de los 8 LEDs
const int buttonPin = 3; // Botón en pin 3

void setup() {
  for (int i = 0; i < 8; i++) {
    pinMode(leds[i], OUTPUT);
  }
  // Configura cada LED como salida
  pinMode(buttonPin, INPUT);
  // Botón como entrada
}

void loop() {
  int buttonState = digitalRead(buttonPin);

  if (buttonState == HIGH) {
    // Encendido progresivo
    for (int i = 0; i < 8; i++) {
      digitalWrite(leds[i], HIGH);
      delay(500);
    }
  } else {
    // Apagado progresivo en orden inverso
    for (int i = 7; i >= 0; i--) {
      digitalWrite(leds[i], LOW);
      delay(500);
    }
  }
}
  
```

Códigos de programación empleados

Figure 2. Programming code used.

RESULTS

The completion of the experimental stages resulted in the consolidation of a functional prototype with the technical capacity to simultaneously emulate the transmission dynamics of star and ring topologies in a controlled hardware environment. This system facilitated the empirical validation of node hierarchy and sequential data packet transit, establishing a direct relationship between theoretical interconnectivity models and the physical behavior of electrical signals [10], [14], [15]. The integration of microcontrollers and peripheral components on a 3,260-point breadboard ensured efficient spatial organization, significantly reducing electromagnetic noise and allowing clear visual monitoring of information flows during signal synchronization tests [12], [13].

Table 2 summarizes the quantitative performance indicators recorded during the functional validation of both prototypes. All functional tests were conducted under controlled laboratory conditions. The 300 ms inter-node delay was deliberately configured to allow human visual perception of the data flow, which in a real network would occur at imperceptible speeds. The system completed all programmed activation sequences without errors across repeated trials, confirming the stability and reliability of the hardware-software integration.

TABLE 2. QUANTITATIVE PERFORMANCE INDICATORS OF THE PROTOTYPE SYSTEM

Indicator	Star topology	Ring topology
Number of nodes simulated	5 (+ 1 central hub)	8
Activation delay per node (ms)	300	300
Total cycle time — full sequence (ms)	~1,500	~2,400
Correct activations / total tests	10 / 10	10 / 10
Failure rate (%)	0	0
Protection resistors per node (Ω)	220	220
Input pull-down resistors ($k\Omega$)	10	10
Digital pins used	5 (pins 2–6)	5 (pins 8–12)
Total implementation cost (COP)	166,500 (combined)	—

In terms of financial viability, the full development of both network configurations required a total investment of 166,500 COP, as detailed in the project budget breakdown. This economic assessment demonstrates that leveraging open hardware platforms enables the creation of high-fidelity pedagogical tools with minimal investment, supporting the implementation of network laboratories in academic contexts with limited resources [11], [13]. The results confirm that the proposed architecture not only meets the logical programming requirements but also offers a sustainable and replicable model for research into communication protocols and electronic agent synchronization using open hardware [12], [14]. (see Figure 3).

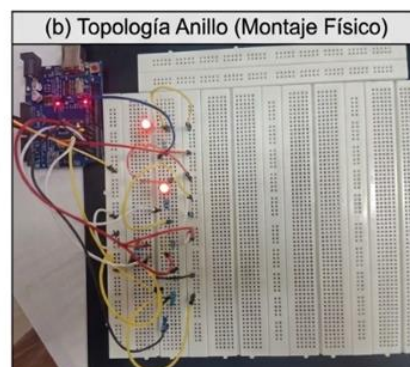
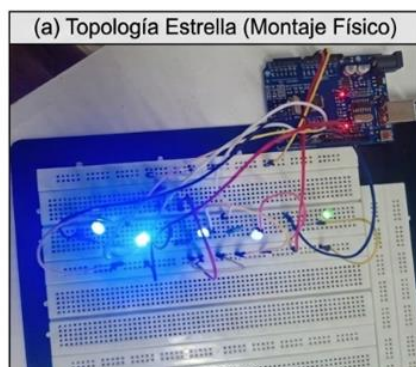


Figure 3. Physical assembly and network topology simulation in hardware. (a) Star Topology: progressive activation of blue LEDs controlled by a central Arduino UNO node. (b) Ring Topology: sequential arrangement of red LEDs mounted on a 3,260-point breadboard, simulating the circular flow of information. Both assemblies integrate protection resistors and push buttons for activation of programming logic.

DISCUSSION

The execution of this research project enabled the work team to consolidate practical knowledge of network topologies in physical environments. While this experience suggests a potential positive impact on the technical competence of participants, its rigorous quantification would require formal evaluation instruments, which constitute part of the future work. The implementation of the open hardware-based prototype is consistent with the postulates of Cognitive Load Theory [10], insofar as the physical representation of concepts allows distributing mental load across visual and tactile channels. However, formal validation of this hypothesis with a student population using standardized instruments remains proposed as a future line of research. This approach is aligned with technical documentation highlighting the ease of learning through direct experimentation with microcontrollers [11], [13].

Regarding the contrast with virtual simulators, it is suggested that direct contact with hardware could complement the use of tools such as Cisco Packet Tracer [10], by exposing students to physical variables that virtual environments do not reproduce. Although simulators allow modeling complex architectures under global theoretical standards [10], they tend to omit critical physical variables such as electromagnetic noise or cable contact failures that can only be perceived in a real breadboard implementation [13], [15]. This hands-on experience allows students to understand that a network is not merely a logical abstraction but a physical infrastructure subject to real electrical and mechanical limitations [11]. A quantitative comparison of the impact of both approaches on learning constitutes a pending research objective.

Regarding perceived latency analysis, direct observation of the sequential LED activation allowed the team to assimilate synchronization concepts and propagation times that two-dimensional graphs in textbooks cannot convey with the same clarity [15]. By adjusting control algorithms, synchronization protocols were validated that ensure data delivery within deterministic timeframes, lending a pragmatic sense to data traffic engineering [12], [14]. This physical visualization of circular or radial information flow facilitates the detection of bottlenecks and latencies that are fundamental in the study of modern high-availability networks [10], [15].

Regarding the impact on problem-solving, encountering connection errors or code failures during physical assembly strengthened the team's analytical capacity and technical resilience [13]. The trial-and-error process inherent in working with open hardware compels the researcher to conduct exhaustive debugging of both software logic and hardware integrity [11], [13]. It is considered that this iterative debugging capacity, inherent to open hardware work, has potential to strengthen analytical skills in students; however, empirical verification would require a comparative study with a control group. This competence is particularly relevant in the development of complex systems where programming logic must correctly interact with passive components and sensors under real operating conditions [11].

Finally, the relationship with international standards underscores that the use of emerging technologies and open educational resources is a global trend for closing digital gaps in economically limited regions [3]. By grounding learning in low-cost tools and open synchronization protocols, a more inclusive engineering education is promoted, aligned with the needs of today's technology industry [12], [14]. The democratization of technical knowledge through hardware simulation not only enhances long-term information retention but also fosters a culture of innovation necessary to address the challenges of telecommunications in the contemporary context [14].

DESIGN AND IMPLEMENTATION OF AN EDUCATIONAL RESOURCE FOR TEACHING NETWORK TOPOLOGIES

CONCLUSIONS

This study successfully designed and implemented an interactive prototype for the physical simulation of star and ring network topologies using Arduino UNO microcontrollers, embedded programming, and low-cost electronic components. The results demonstrated that the developed system adequately fulfilled its stated purpose, functionally, visually, and sequentially representing the basic structural behavior of both network architectures.

Experimental validation confirmed that the prototype performed stably during operational tests, correctly executing the programmed activation sequences and clearly reproducing the communication logic associated with each topology. In particular, the star topology evidenced the dependency of multiple nodes on a central controller, while the ring topology satisfactorily reproduced the continuous sequential circulation of information between interconnected nodes.

From an educational perspective, the developed prototype represents a didactic proposal with potential to support the practical understanding of abstract computer networking concepts, by offering a visual, physical, and interactive learning experience. However, the verification of the actual impact on student learning was not within the scope of this study and should be addressed through future research with experimental design. Likewise, the interdisciplinary nature of the prototype facilitated the integration of knowledge related to basic electronics, programming, and network architecture within a single experimental environment.

Finally, the low cost, functional stability, and ease of replication of the developed system demonstrate that the proposed prototype constitutes a viable tool for implementation in academic environments focused on the teaching of networks and embedded systems. As future work, the following is proposed: (1) expand the experimental architecture toward the simulation of more complex topologies such as mesh and tree; (2) design a quasi-experimental study with a control group and an experimental group to measure the pedagogical impact of the prototype through pretest/posttest assessments and validated satisfaction instruments; and (3) explore the integration of wireless communication modules to simulate networks closer to real-world environments.

AUTHOR CONTRIBUTION

The author's contributions to this article are as follows:

Sara Sofía Conde Barrios: Conceptualization, Methodology, Investigation, Validation, Formal analysis, Writing—original draft, Writing—review and editing.

Yudis Del Carmen Franco Ariza: Conceptualization, Investigation, Data curation, Formal analysis, Visualization, Writing—original draft, Writing—review and editing.

José David Garrido Martínez: Methodology, Software, Hardware implementation, Validation, Investigation, Data curation, Visualization, Writing—original draft.

Kenderson Guerrero Rodríguez: Software, Hardware implementation, Validation, Investigation, Formal analysis, Visualization, Writing—original draft.

Carlos Arnulfo Garzón Mercado: Supervision, Project administration, Methodology, Validation, Formal analysis, Writing—review and editing.

The author reviewed the results and approved the final version of the article.

CONFLICT OF INTERESTS

The authors declare that they have no interests or financial relationships that could have influenced this work.

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DATA AVAILABILITY STATEMENT

The Arduino source code and hardware configuration supporting the results of this study are openly available on GitHub at: <https://github.com/766ms/Topologias-Anillo-y-Estrella-CURN.git>

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